REMARKS

Applicants have amended the claims to more particularly define the invention taking into consideration the outstanding Official Action. The limitation of claims 24 and 33 have been respectively added to claims 20 and 29. Claims 24 and 33 have been canceled from the application. The claims remaining in the application are claims 20-23, 25-28 and 30 -39. Applicants most respectfully submit that all of the claims now present in the application are in full compliance with 35 USC 112 and are clearly patentable over the references of record.

The rejection of claims 20-28, 37 and 39 under 35 U.S.C. 103(a) as being unpatentable over Scott et al. in view of Matsuoka et al. and Sugiyama et al. has been carefully considered but is most respectfully traversed in view of the amendments to the claims Applicants wish to direct the Examiner's attention to the basic requirements of a prima facie case of obviousness as set forth in the MPEP § 2143. This section states that to establish a prima facie case of obviousness, three basic criteria first must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Section 2143.03 states that all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Applicants also most respectfully direct the Examiner's attention to MPEP § 2144.08 (page 2100-114) wherein it is stated that Office personnel should consider all rebuttal argument and evidence present by applicant and the citation of In re Soni for error in not considering evidence presented in the specification.

With respect to claim 20, it is urged in the Official Action that Scott et al. show a substrate 10, a phototransistor 250, a bipolar transistor 260 with collector layer 30, 40, base layer 60, emitter layer 90, 100 and distinct mesas which are formed and are separated by a space which provides insulation. These are said to be formed on a single substrate. It is further noted that the Scott et al. device is a high speed device and is intended for edge illumination.

The Official Action also states that Matsuoka et al. show a similar device which is intended for top illumination. It is concluded that it would have been obvious to use the Matsuoka et al. structure in the Scott et al. device for a top illumination device to provide the structure for a different application. However, Applicants most respectfully submit that the necessary motivation to make this modification is not found in the prior art. This is especially true since the teaching is to provide a different application. What different application. That taught by applicant?. The only motivation for this modification is found in Applicants' disclosure which is not a viable teaching reference to provide a tenable rejection under 35 U.S.C. 103(a).

Applicants wish to emphasize a system-on-chip (SOC) technology combining a silicon germanium photodetector (SiGe photodetector) and a high-speed IC, having characteristics of producing adjustable, high-response SiGe photodetector and high-speed SiGe transistor in a single manufacturing process by adding a light absorbing layer on the SiGe photodetector collector zone is unobvious. Even if the cross sectional charts for both elements are the same, this transistor photodetector has characteristics of reducing the complexity of manufacturing, high-responding and varying the wavelength sensitivity selection by changing the content of Germanium. This drastically increases the functionality of the detector and thus is very suitable to be used in a high-

speed optical fiber/optical wave-guide communication network system with excellent results.

Scott et al. discloses the usual HBT (Heterojunction Bipolar Transistor) structures Phototransistor, no light absorbing layer is added. The presently claimed invention discloses a SiGe Light Absorbing Layer added on the collector layer of the SiGe HBT structure, without affecting the characteristic of high-responding thereof. Since the premise is different and the '925 reference does not disclose a light absorbing layer, the presently claimed invention cannot be considered as obvious, even if some parts of the instant invention overlap the '925 reference.

Matsuoka et al. and the presently claimed invention are grouped in OEICs (Optical-Electronic Integrated Circuits), the scope of the claims disclosed are different and unobvious. The photodetector of the '117 patent is a P-i-N structure, different from MQW's (Multiple Quantum Wells) or SLs disclosed in the presently claimed invention as would be appreciated by one of ordinary skill in the art to which the invention pertains. The manufacturing of P-i-N is complex and has the disadvantage of reducing the characteristic of high responding of the high-speed transistor, as compared with the instant invention. The method to achieve the wavelength selection capability is different as well (changing the materials of semiconductor film of '117 compare with changing contents of Germanium).

Sugiyama et al. – the SiGe SLs (Superlattices) structured photodetector of the '860 does not amplify the photoelectric current and does not have high-response capability. Further, the optical elements and electronic elements are built separately in sequence. However, the optical and electronic elements are built together in the same processing in the presently claimed invention. This results in a huge improvement in the view of device physics and process technology.

The data obtained from the experiments run under the concept of the presently claimed invention can be found in enclosures, and the relevant article has been published in IEDM (International Electron Device Meeting) year 2002 as well. Accordingly, it is most respectfully requested that the rejection be withdrawn.

The rejection of claims 29-36 under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al. in view of Sugiyama et al. has been carefully considered but is most respectfully traversed for the reasons discussed above. A prima facie case of obviousness has not been established because the necessary motivation to modify the teachings of the references in the expectation of arriving at the claimed invention is not present.

In the Official Action it is urged that with respect to claim 29, Matsuoka et al. show a bipolar/detector device on a single substrate, which is intended for top illumination and uses layers 7, 7a as absorption layers with 3, 4, 5 and 6 being part of the collector and has and base 8 and emitter 9. Sugiyama et al. is relied upon to show that a related structure can be formed with a silicon substrate and uses SiGe since SiGe can be used to select the wavelength of sensitivity and uses an inexpensive silicon process. It is conclude that it would have been obvious to use the Sugiyama et al. material to achieve the wavelength selection capability and the use of inexpensive processing. Note also that Sugiyama et al. show that recombination at the end faces of a mesa can cause recombination and therefore uses a dielectric insulation 5.

As just noted Matsuoka et al. and the presently claimed invention are grouped in OEICs (Optical-Electronic Integrated Circuits), the scope of the claims disclosed are different and unobvious. The photodetector of the '117 patent is a P-i-N structure, different from MQW's (Multiple Quantum Wells) or SLs disclosed in the presently claimed invention as would be appreciated by one of ordinary skill in the art to which the invention pertains. The manufacturing of P-i-N is complex and has the disadvantage of reducing the characteristic of high responding of the high-speed transistor, as compared with the instant invention. The method to achieve the wavelength selection capability is different as well (changing the materials of semiconductor film of '117 compare with changing contents of Germanium).

Sugiyama et al. – the SiGe SLs (Superlattices) structured photodetector of the '860 does not amplify the photoelectric current and does not have high-response

capability. Where is the motivation to combine the references and arrive at the claimed invention. It simply is not in the prior art.

Further, the optical elements and electronic elements are built separately in sequence. However, the optical and electronic elements are built together in the same processing in the presently claimed invention. This results in a huge improvement in the view of device physics and process technology.

The data obtained from the experiments run under the concept of the presently claimed invention can be found in enclosures, and the relevant article has been published in IEDM (International Electron Device Meeting) year 2002 as well. Accordingly, it is most respectfully requested that the rejection be withdrawn.

Again, Applicants most respectfully submit that this rejection is based upon hindsight reconstruction of the references and should be withdrawn.

In view of the above comments and further amendments to the specification and claims, favorable reconsideration and allowance of all of the claims now present in the application are most respectfully requested.

Respectfully submitted,

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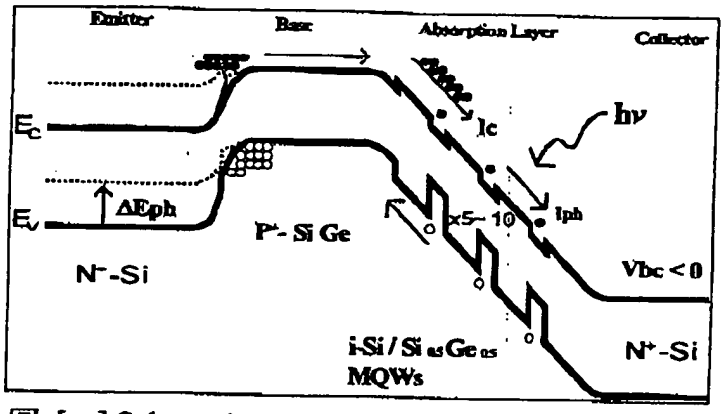

圖 [一] Schematics of SiGe phototransistor operation

表 [一] Comparison of ERSO's SiGe PHT with other detector

Company	Technology	Responsivity (A/W)	Bandwidth (GHz/Gbps)	RxBW (GhzxA/W)	Voltage (Volts)	Dark current
OSI	Si PIN	0.26	2.5	0.65	3.3	10 pA
EMCORE	GaAs	0.5	10	5	1.6	0.2 nA
OPTO Speed	InGaAs	0.45	5	2.25	2	10nA
ERSO*	SiGe	0.43 17.5	3 0.5	1.3 8.75	0.5~3V	100pA
IBM	Si SOI	0.35 0.08	2 10	0.7 0.8	3.3	30 uA

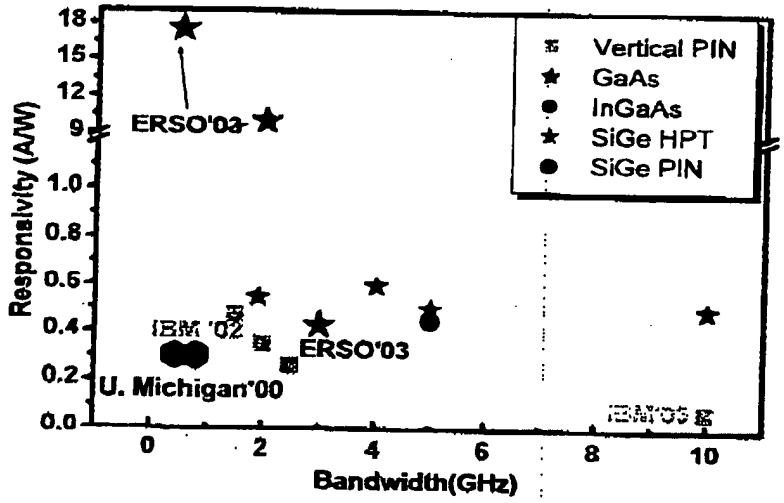

圖 [二] Comparison of ERSO's SiGe PHT with other detector in term of bandwidth and resposibility